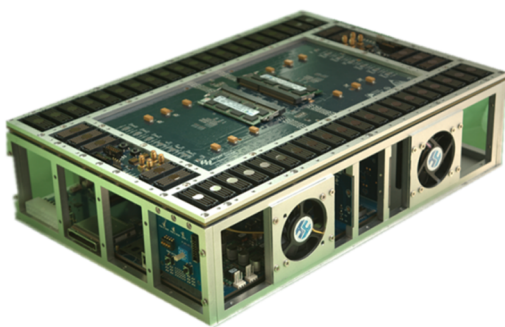


Supernova-DH4000T

SOC/IP FPGA Prototyping Board

DESIGN² For Your DESIGN



Supernova-DH4000T

- Supernova Series FPGA prototyping board provides Rapid Prototyping Platform for various types of digital circuit design, greatly shortening the development cycle of SOC / IP and FPGA.
- Supernova-DH4000T series of validation board provides up to two Xilinx ® UltraScale XCVU440, supporting up to 80 million logic gates design verification, applicable to a variety of communications, multimedia and consumer SOC / IP prototyping and various algorithms.
- Separate extension interfaces, in line with the HSPI2 [High Speed Prototyping Interface2] provide users long-term expandability, up to 2120 GPIOs.
- Extension interface with HSPI2-GTX[High Speed Prototyping Interface2-Transceiver],Supply PCI-e 3.0;SATA;SFP+;Rapid I/O etc. High Speed Transceiver interface.
- Structured power module, control module, the function module. Can be very convenient to realize the extension system, the system structure of transplant, can maximize the prototype verification platform flexibility into full play.
- ProtoWizard-DH4000T Software Support. Can supply ‘System monitor’; ‘System Configuration’; ‘Rapid IO Pin Mapping’.

Supernova-DH4000T • System prototype board

Radrix Co., Ltd.

Incubation Facility Kyushu Institute of Technology
680-4, Kawazu, Iizuka, Fukuoka,
Japan 820-8502
Tel: 81-948297937 Fax: 81-948297692 <http://www.radrix.com>

Features

- The largest of Logic Capacity - based on Xilinx UltraScale-XCVU440 FPGA with 8M Logic Elements, 177.2Mb Block RAM, capable for a maximum 80M ASIC gates.
- Xilinx All Programmable Zynq for FPGA/Clock configuration/programming, voltage and system monitoring and control.
- Structured power module, control module, the function module.
- There are two types of DDR3-SODIMM Socket supports 4GByte DDR3 Memory Capacity. Reserved for DDR4 Expansion.
- Separate extension interfaces, in line with the HSPI2 [High Speed Prototyping Interface2] provide users long-term expandability, up to 2120 GPIOs.
- Extension interface with HSPI2-GTX[High Speed Prototyping Interface2-Transceiver],Supply PCI-e 3.0;SATA;SFP+;Rapid I/O etc. High Speed Transceiver interface.
- Inter-Connection with 100 Pairs of LVDS+1Quad Transceiver I/O.
- All HSPI2 interface independent Bank connection, can provide 51 GPIOs, through the GUI software configuration, can achieve 1.2 V,1.35 V,1.5 V,1.8 V Bank voltage is adjustable.
- Two OSC Global Clocks and Two Differential Input Clocks.
- Independent Clock Output X 162 pairs; Special Clock Input X2 used for DDR3;Shared Clock Input X8 pairs; GTX Clock Input X24 pairs; GTX Clock Output X 20 Pairs.
- FPGA Configuration Methods consist of :USB, Remote Ethernet Configuration, SD Card,JTAG
- Support UART interface, BCD, RTC, EEPROM, LEDs, Resets, Switches
- Automatic Threshold Alarms
- Automatic Voltage/Current/Temperature Monitors
- Smart Fan Control
- ATX Power Supply
- ISO9000 Standard Assembly
- ProtoWizard Support Windows and Linux OS.

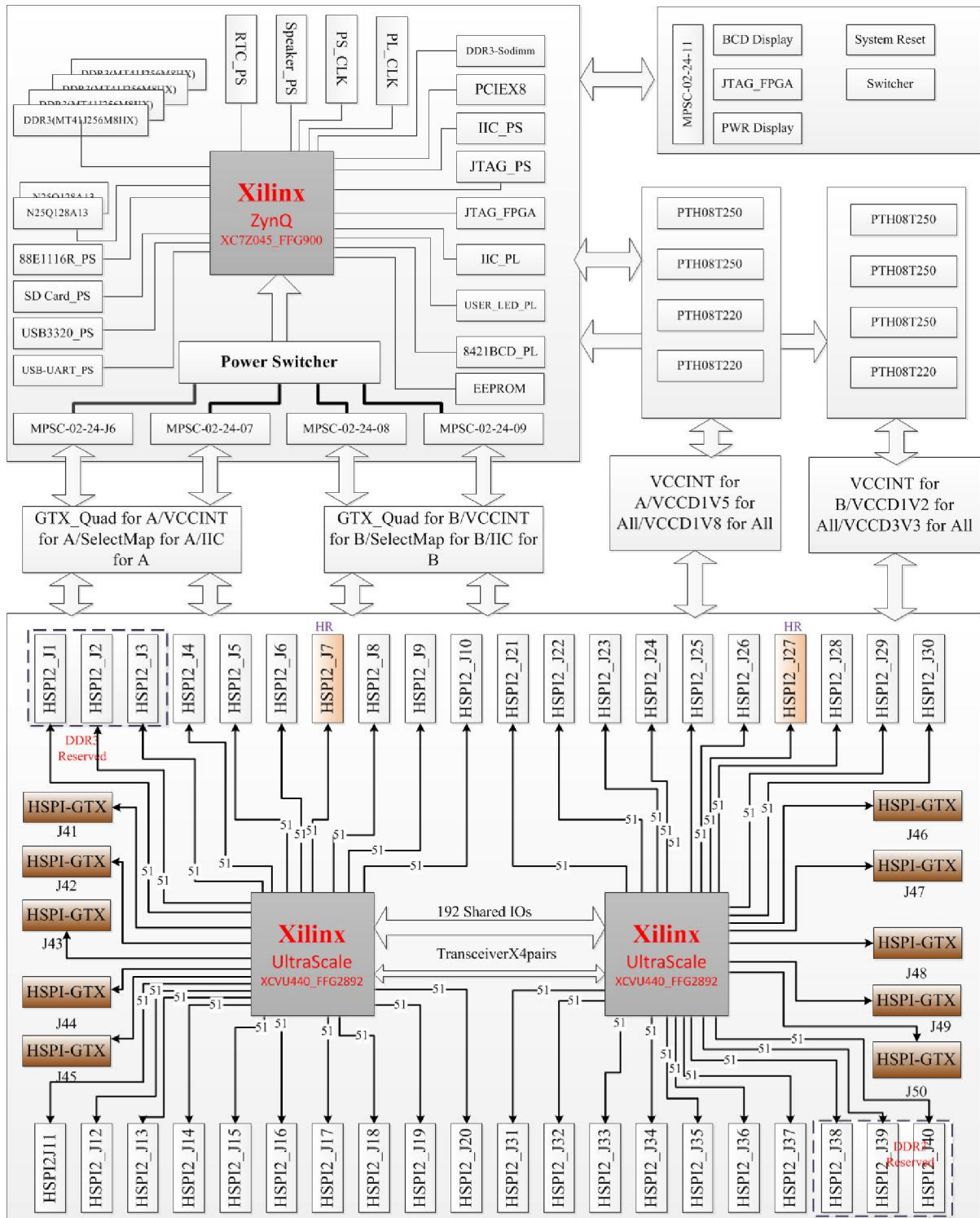
Expansion Boards

- DDR4 SODIMM Daughter Card
- LPDDR/LPDDR2/LPDDR3 Daughter Card
- NOR FLASH Daughter Card
- NAND FLASH Daughter Card
- UART Daughter Card
- Analog video input and output sub-board
- Analog audio input and output sub-board
- HDMI &DVI video input daughter board
- LCD interface
- CCD/CMOS imaging sensors
- DVI Input / Output daughter board
- 100M/1000M Ethernet PHY
- USB 1.1/2.0/OTG PHY
- USB Interface
- PS2 HID Interface
- TS stream input and output interface
- Mobile-DDR Daughter Card



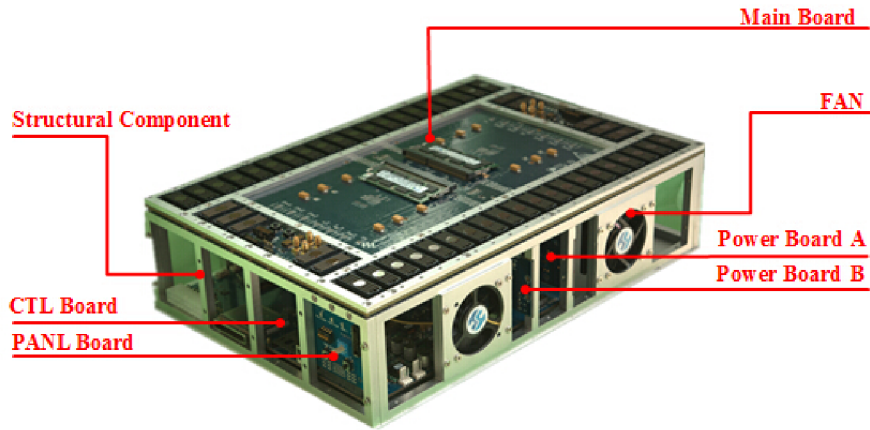
Supernova-DH4000T • System prototype board

System Structure Diagram

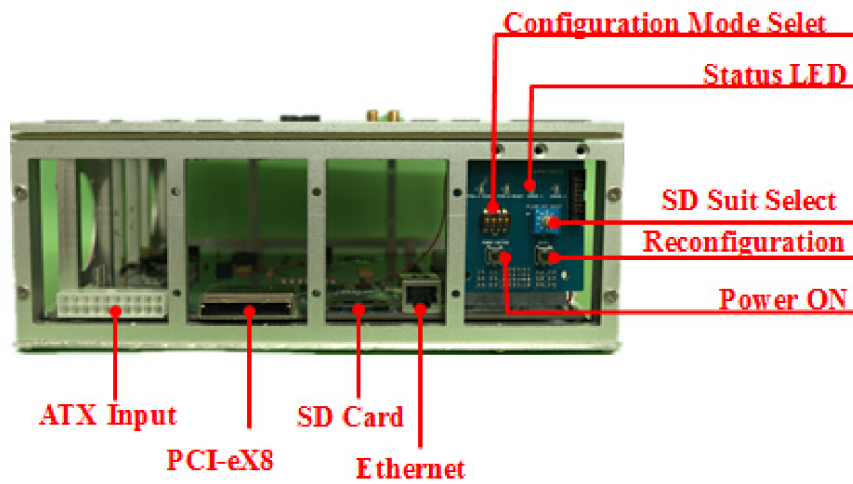


Supernova-DH400T • System prototype board

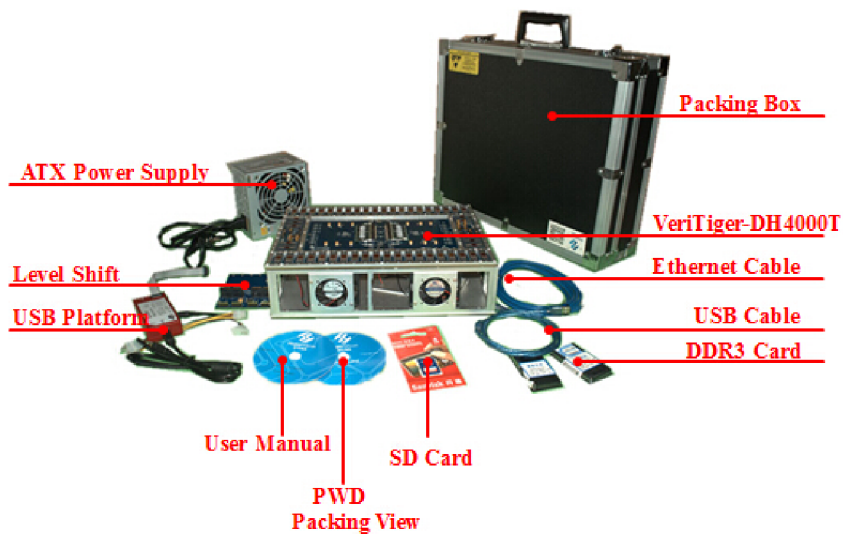
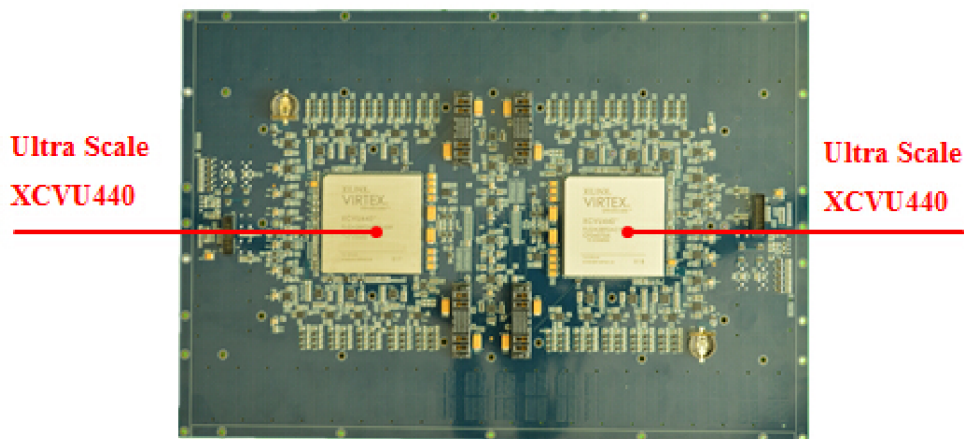
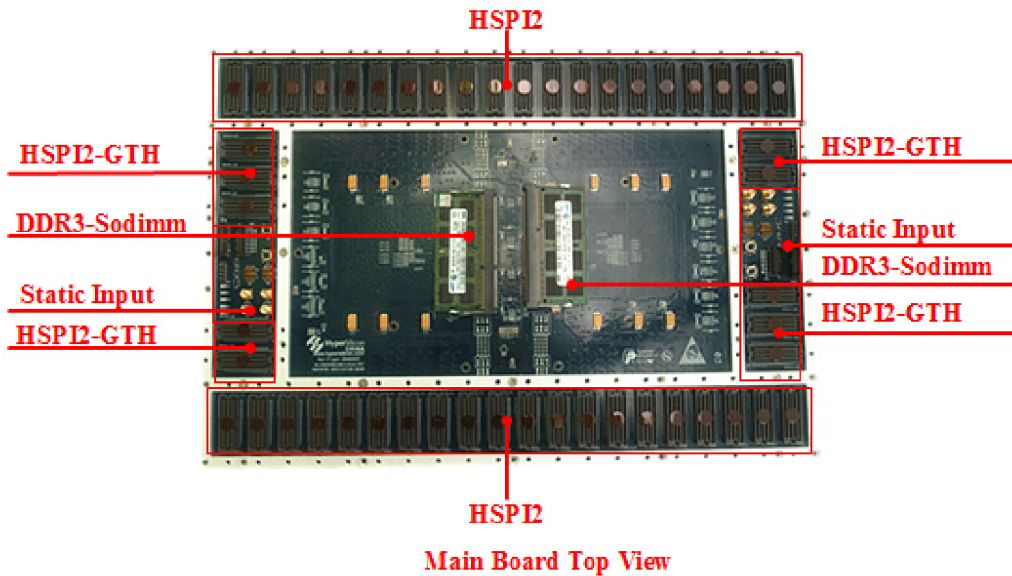
Board View



45 Degree View



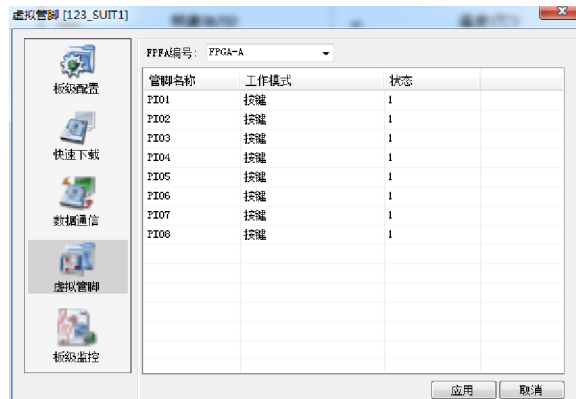
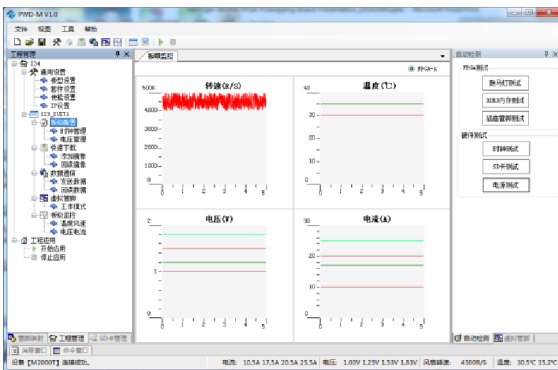
Lateral View



Available demo

- JTAG/Ethernet/SD Card Loading
- LEDs, Reset, DIP Switch Configuration
- DDR3 W/R Test Demo
- PCI-E Endpoint Test Demo
- Partition by TDM

Debug Tool -ProtoWizard



- **System Configuration**

- Loading image file by USB
- Loading image file by Remote Ethernet
- Multiplex system clock configuration, read back
- Configuration Image address Settings, read back

- **System Testing**

- FPGA Initial testing
- Socket IO automatic testing
- External memory automatic testing
- system clock Automatic testing
- SD card to start the function testing
- System of power Automatic test

- **Data Communication:**
 - Through the USB interface to realize the FPGA test data communication with operating system
 - Through the Ethernet interface test data communication with operating system
- **Virtual I/O s:**
 - 8 Units Virtual LED
 - 8 Units Virtual Switcher
 - 8 Units Virtual Pushing Buttons

Ordering Information

Model	No. of FPGAs	FPGA Model
威虎(Supernova)-DH4000TC1	2	Xilinx UltraScale XCVU440—FLG2892C1
威虎(Supernova)-DH4000TC1L	1	Xilinx UltraScale XCVU440—FLG2892C1
威虎(Supernova)-DH4000TC1R	1	Xilinx UltraScale XCVU440—FLG2892C1
威虎(Supernova)-H4000TC1	1	Xilinx UltraScale XCVU440—FLG2892C1
威虎(Supernova)-DH4000TC2	2	Xilinx UltraScale XCVU440—FLG2892C2
威虎(Supernova)-DH4000TC2L	1	Xilinx UltraScale XCVU440—FLG2892C2
威虎(Supernova)-DH4000TC2R	1	Xilinx UltraScale XCVU440—FLG2892C2
威虎(Supernova)-H4000TC2	1	Xilinx UltraScale XCVU440—FLG2892C2

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